Lab 2: MIPS Datapath for R-type Instructions

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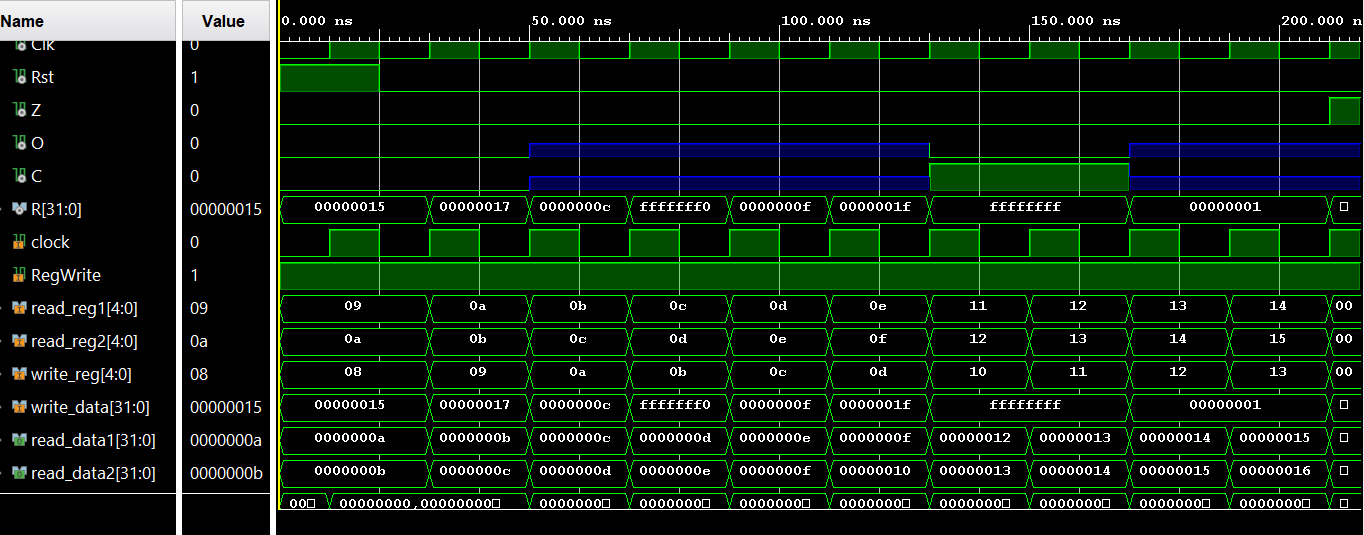
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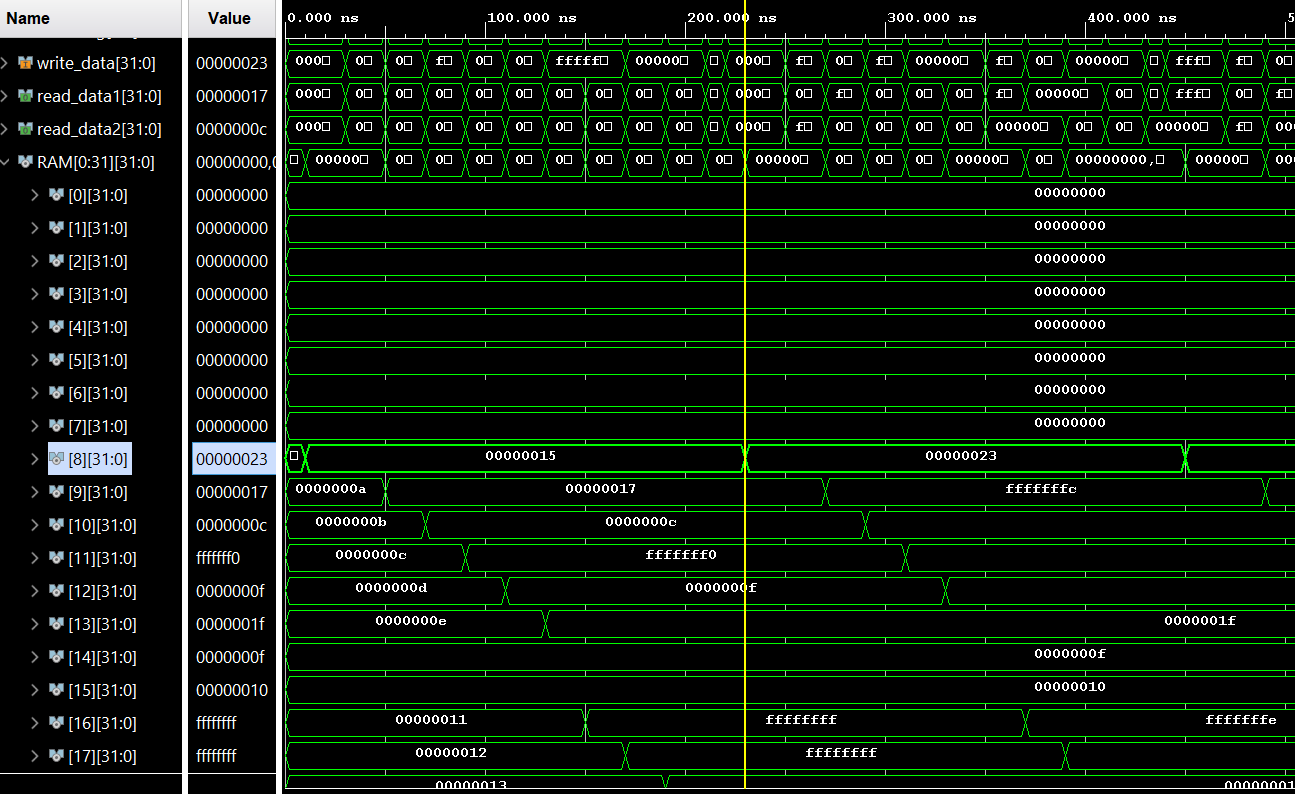
06.25.2020

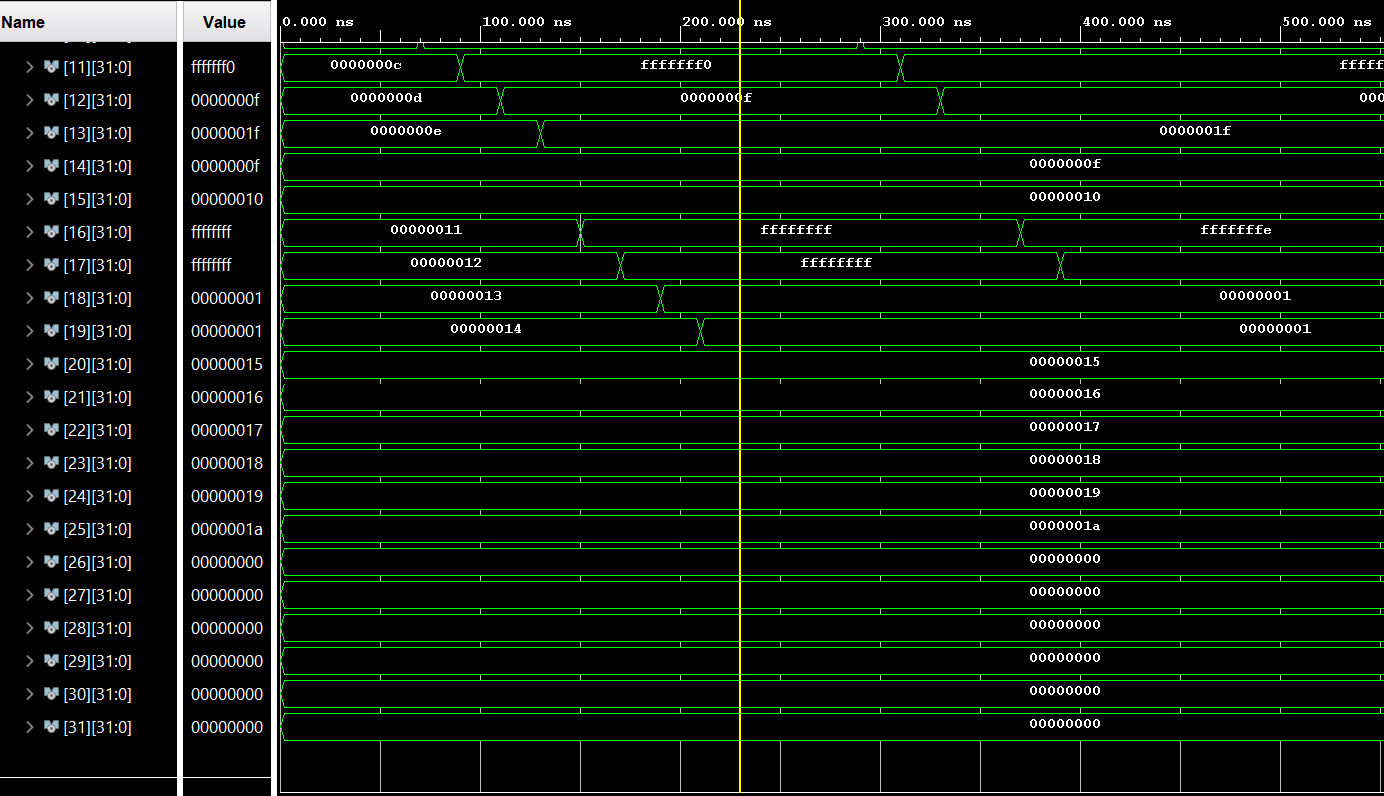
**Introduction:** The purpose of this lab is to construct a MIPS Datapath for R-type instructions using VHDL. The idea is that the basic inputs of clock and reset will produce a 32-bit output.

**Problem Logic & Solution:** Vivado’s block design tool was used to construct a block design that could process R-type instructions.

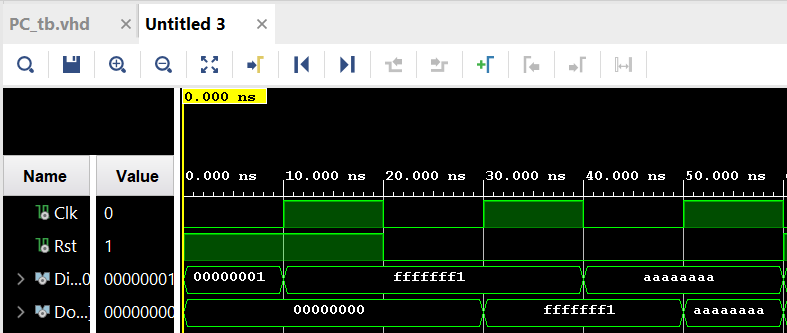
* Simulation Results



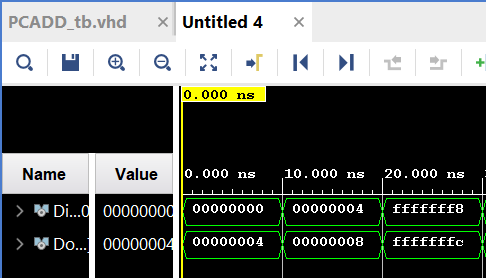




* PC Simulation Result



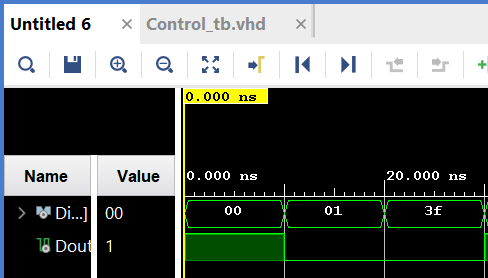
* PCADD Simulation Result

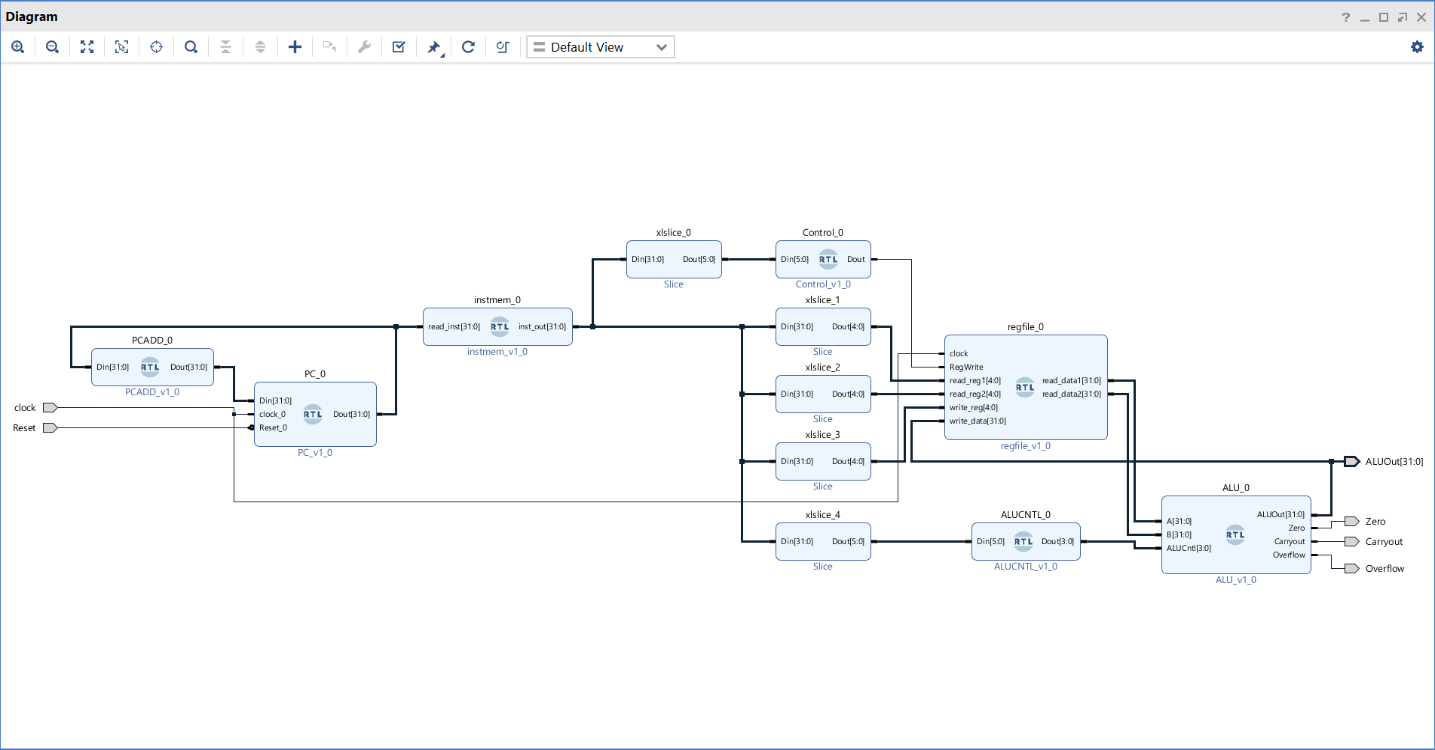


* ALUCNTL Simulation Results



* Control Simulation Results



* Block Design Snapshot

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No | Register | Calculated [Hex] | | Simulated [Hex] | |
| Initial Value | Final Value | Initial Value | Final Value |
| 0 | $zero | 00000000 | 00000000 | 00000000 | 00000000 |
| 1 | $at | 00000000 | 00000000 | 00000000 | 00000000 |
| 2 | $v0 | 00000000 | 00000000 | 00000000 | 00000000 |
| 3 | $v1 | 00000000 | 00000000 | 00000000 | 00000000 |
| 4 | $a0 | 00000000 | 00000000 | 00000000 | 00000000 |
| 5 | $a1 | 00000000 | 00000000 | 00000000 | 00000000 |
| 6 | $a2 | 00000000 | 00000000 | 00000000 | 00000000 |
| 7 | $a3 | 00000000 | 00000000 | 00000000 | 00000000 |
| 8 | $t0 | 00000009 | 00000015 | 00000009 | 00000015 |
| 9 | $t1 | 0000000A | 00000017 | 0000000A | 00000017 |
| 10 | $t2 | 0000000B | 0000000C | 0000000B | 0000000C |
| 11 | $t3 | 0000000C | FFFFFFF0 | 0000000C | FFFFFFF0 |
| 12 | $t4 | 0000000D | 0000000F | 0000000D | 0000000F |
| 13 | $t5 | 0000000E | 0000001F | 0000000E | 0000001F |
| 14 | $t6 | 0000000F | 0000000F | 0000000F | 0000000F |
| 15 | $t7 | 00000010 | 00000010 | 00000010 | 00000010 |
| 16 | $s0 | 00000011 | FFFFFFFF | 00000011 | FFFFFFFF |
| 17 | $s1 | 00000012 | FFFFFFFF | 00000012 | FFFFFFFF |
| 18 | $s2 | 00000013 | 00000001 | 00000013 | 00000001 |
| 19 | $s3 | 00000014 | 00000001 | 00000014 | 00000001 |
| 20 | $s4 | 00000015 | 00000015 | 00000015 | 00000015 |
| 21 | $s5 | 00000016 | 00000016 | 00000016 | 00000016 |
| 22 | $s6 | 00000017 | 00000017 | 00000017 | 00000017 |
| 23 | $s7 | 00000018 | 00000018 | 00000018 | 00000018 |
| 24 | $t8 | 00000019 | 00000019 | 00000019 | 00000019 |
| 25 | $t9 | 0000001A | 0000001A | 0000001A | 0000001A |
| 26 | $k0 | 00000000 | 00000000 | 00000000 | 00000000 |
| 27 | $k1 | 00000000 | 00000000 | 00000000 | 00000000 |
| 28 | $gp | 00000000 | 00000000 | 00000000 | 00000000 |
| 29 | $sp | 00000000 | 00000000 | 00000000 | 00000000 |
| 30 | $fp | 00000000 | 00000000 | 00000000 | 00000000 |
| 31 | $ra | 00000000 | 00000000 | 00000000 | 00000000 |

**Conclusion:** My calculated results matched my simulated results leading me to conclude the lab was done successfully. Please note in the Lab 2 folder I am providing there are multiple testbench files one for the Datapath and four for the components.